CUSTOMIZABLE DEVELOPMENT AND DEMONSTRATION PLATFORM FOR STRUCTURED ASICS

ABSTRACT

The present invention is directed to a customizable development and demonstration platform for structured ASICs. In an exemplary aspect of the present invention, the present platform may include a structured ASIC which is built on a slice and which may be flexible enough for a number of possible application developments. This flexibility may be achieved by incorporating a programmable processor in the structured ASIC and by defining interfaces and the use of an external FPGA in the present platform. The structured ASIC may include a complete ARM processor subsystem and a plurality of high speed SERDES ports. The processor subsystem may include a bus interface to the external FPGA, allowing custom gate development and test in the FPGA, prior to incorporating it into the customer product. Through the SERDES ports, the test block may be used to show the electrical characteristics of the SERDES IP. In addition, some SERDES ports may be driven from a link layer realized in the FPGA. This may allow the same chip and board to implement SATA (serial advanced technology attachment), GigE, XAUI, XGXS, Fibre Channel, and the like by changing the programming of the FPGA on the board.